What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a plurality of dopant pockets on a substrate comprising:

forming a plurality of implantable regions on said substrate separated by field oxide regions, said implantable regions and field oxide regions extending in a first direction;

forming a plurality of word lines located over said implantable regions and field oxide regions, said word lines extending in a second direction perpendicular to said first direction;

removing portions of said field oxide regions between two adjacent word lines to expose respective substrate regions;

forming source regions in said implantable regions; and

implanting a dopant into said substrate through said respective substrate regions to form said dopant pockets beneath said source regions.

2. The method of claim 1, wherein said dopant is a p-type dopant.

3. The method of claim 1, wherein said dopant is boron.

4. The method of claim 1, wherein said dopant is BF_2.

5. The method of claim 1, wherein said dopant is an n-type dopant.

6. The method of claim 1, wherein said act of removing portions of said field oxide regions further comprises selectively etching said portions of field oxide regions relative to said substrate and said word lines.

7. The method of claim 1, wherein each of said word lines is formed of a gate stack comprising a gate oxide, a floating gate, a dielectric formed over said floating gate, and a control gate formed over said dielectric.

8. The method of claim 1, wherein said act of implanting said dopant into said substrate is carried out after said act of forming said source regions.

9. The method of claim 8, wherein said act of implanting said dopant is carried out with an implanting energy higher than implanting energy used to form said source regions.

10. The method of claim 9, wherein said act of implanting said dopant employs directing said dopant through said substrate region at an angle of substantially 90 degrees incidence to said substrate region.

11. The method of claim 9, wherein said act of implanting said dopant employs directing said dopant through said substrate region at angles different than substantially 90 degrees incidence to said substrate region.

12. The method of claim 7, wherein said act of implanting said dopant into said substrate is carried out after said act of forming said source regions.

13. A method of forming source regions with boron pockets on a substrate of a flash memory, said method comprising:

forming a field oxide layer over said substrate;

forming a pair of adjacent spaced word lines over said field oxide layer;

removing said field oxide layer from predefined regions located in between said spaced word lines to expose respective substrate regions;

forming a source region in between said word lines; and

implanting boron into said substrate in between said word lines to form a boron pocket beneath said source region.

14. The method of claim 13, wherein said act of implanting boron into said substrate is carried out after said act of removing said field oxide material.

15. The method of claim 14, wherein said act of implanting boron into said substrate is carried out after said act of forming said source region.

16. The method of claim 15, wherein said act of implanting boron is carried out at with an implanting energy higher than an implanting energy for said source region.

17. The method of claim 16, wherein said act of implanting boron employs directing boron through said substrate region at an angle of substantially 90 degrees incidence to said substrate region.

18. The method of claim 16, wherein said act of implanting boron employs directing boron through said substrate region at angles different than substantially 90 degrees incidence to said substrate region.

19. The method of claim 14 wherein the act of implanting boron into said substrate is carried out before said act of forming said source region.

20. A method of forming a source region in a substrate comprising:

forming a pair of gate structures which extend in a first direction over a substrate;

altering the upper surface profile of said substrate to form alternating areas of higher substrate surface elevation and areas of lower substrate surface elevation along said first direction and between said pair of gate structures;

providing a first doped layer in said substrate between said gate structures which has a profile which follows that of said upper surface profile; and

providing a second doped layer in said substrate between said gate structure which is below said first doped layer and which has a profile which follows that of said first doped layer.

21. The method of claim 20, wherein at least one of said areas of higher and lower substrate surface elevation is doped by said first doped layer to act as a source region of a transistor.

22. The method of claim 21, wherein said area of higher substrate surface elevation acts as said source region.

23. The method of claim 20, wherein said first doped layer is provided in said substrate before said second doped layer.

24. The method of claim 20, wherein said second doped layer is provided in said substrate before said first doped layer.

25. A semiconductor device comprising:

a substrate including a region doped to provide a source region for at least one transistor, said substrate having an upper surface which varies in elevation and said source region having a profile which varies in accordance with the variations in said upper surface; and

an implanted region located below and around said source region, said implanted region having a profile that follows that of said source region.

26. The semiconductor device of claim 25, wherein said implanted region forms a pocket around said source region.

27. The semiconductor device of claim 25, wherein said source region is a self-aligned region.

28. The semiconductor device of claim 27, wherein said implanted region is a self-aligned implanted region.

29. The semiconductor device of claim 28, wherein said implanted region is implanted with a p-type dopant.

30. The semiconductor device of claim 29, wherein said p-type dopant is boron.

31. The semiconductor device of claim 29, wherein said p-type dopant is BF_2.

32. The semiconductor device of claim 28, wherein said implanted region is implanted with an n-type dopant.

33. The semiconductor device of claim 25, wherein the thickness of said implanted region is greater than that of said source region.

34. A memory device comprising:

a floating gate formed over a semiconductor substrate between a source region and a drain region;

a control gate formed over said floating gate; and

a self-aligned dopant implanted region located underneath and around said source region.

35. The memory device of claim 34, wherein said self-aligned dopant implanted region includes a p-type dopant.

36. The memory device of claim 35, wherein said p-type dopant is boron.

37. The memory device of claim 35, wherein said p-type dopant is BF_2.

38. The memory device of claim 34, wherein said self-aligned source implanted region has a configuration that follows that of said source region.

39. The memory device of claim 34, wherein said memory device is a flash memory device.

40. The memory device of claim 34, wherein said self-aligned dopant implanted region includes an n-type dopant.

41. A memory structure comprising:

a substrate;

a plurality of spaced field oxide regions provided over said substrate, said spaced field oxide regions extending in a first direction and being segmented at predetermined regions over said substrate;

a plurality of spaced gate stacks extending over said field oxide regions and substrate in a second direction substantially perpendicular to said first direction;

predetermined pairs of adjacent spaced gate stacks having a source region between them extending in said second direction, said predetermined regions residing between said predetermined pairs of adjacent gate stacks, and said source region extending along said predetermined regions; and

an implanted region beneath and extending along said source region.

42. The memory structure of claim 41, wherein said implanted region is a boron implanted region.

43. The memory structure of claim 41, wherein said implanted region forms a pocket for said source region.

44. The memory structure of claim 41, wherein said predetermined regions of said substrate are at a lower substrate surface elevation than other regions of said substrate.

45. The memory structure of claim 44, wherein said source region has a doping profile which follows variations in substrate surface elevation in said second direction.

46. The memory structure of claim 45, wherein said implanted region has a doping profile which follows a doping profile of said source region in said second direction.

47. The memory structure of claim 41 further comprising drain regions located on opposite sides of each of said gate stacks of said predetermined pairs from said source region, said drain regions having portions of said field oxide regions on opposite sides thereof in said second direction.

48. The memory structure of claim 47, wherein said gate stacks, source region and drain regions form a plurality of transistors.

49. The memory structure of claim 48, wherein said transistors are flash memory transistors.

50. The memory structure of claim 41 further comprising a processor coupled to said memory structure.